MOS POWER DEVICE WITH HIGH INTEGRATION DENSITY AND MANUFACTURING PROCESS THEREOF

PRIORITY CLAIM

[1] This application claims priority from European patent application No. 03425099.3, filed February 21, 2003, which is incorporated herein by reference.

TECHNICAL FIELD

[2] The present invention relates to a MOS power device with high integration density and to the manufacturing process thereof.

BACKGROUND

[3] As is known, MOS power devices have the need to form metal regions with low contact resistances on the front of the chip both on P-type regions (body regions) and on N-type regions (source regions). In fact, two of the fundamental characteristics for good operation of a MOS power transistor are the output resistance (Ron) and the direct voltage drop on the body-drain internal diode (Vf).

[4] For a better understanding of the problems involved, reference may be made to **FIG. 1**, which illustrates a perspective cross-sectional view of a known MOS power transistor. In detail, the transistor is formed in a body ***1*** of semiconductor material comprising an N^+-type substrate ***2*** and an N^--type epitaxial layer ***3***. P-type body regions ***4*** extend within the epitaxial layer ***3*** and house N^+-type source regions ***5***. A rear metal region 7 extends on the back of the wafer, in contact with the substrate ***2***.

[5] Gate regions ***10***, of polysilicon, extend on top of the body ***1*** and are electrically insulated from the latter by gate-oxide regions ***11***. The body regions ***4*** extend between adjacent gate regions ***10***, and two source regions ***5*** housed in two different body regions ***4*** extend along the edges of each gate region ***10***. Intermediate-dielectric regions ***12*** cover the gate regions ***10*** both at the top and at

the sides. A source metal region ***13***, shown only partially for clarity, covers the surface of the body ***1*** and, on top of the body regions ***4***, electrically connects the body region ***4*** with the source regions ***5*** housed therein.

[6] The portions of body regions ***4*** underneath the gate regions ***10*** (between each source region ***5*** and the edge of the body region ***4*** facing it) form channel regions ***14***.

[7] To have low contact resistances, it is necessary to heavily dope both the N-type surface regions (source regions ***5***) and the P-type surface regions (body regions ***4***) in contact with the source metal region ***13***. The need for heavy doping of these regions gives, however, rise basically to two different problems.

[8] A first problem is linked to the annealing processes subsequent to the implantation process and to their compatibility with the "scaled" thermal processes employed, for instance, in the manufacture of low-voltage submicrometric devices integrated in the same wafer.

[9] The second problem is linked to the need to have low threshold voltages (1-2 V or even less) and hence low concentrations in the channel regions and, at the same time, high doping levels in the surface regions in contact with the metal regions.

[10] In particular, in this regard, carrying out of an additional implantation for enrichment of the surface of the body regions ***4*** and of the source regions ***5***, through the windows in the polysilicon layer that forms the gate regions ***10***, would affect the surface concentration of the channel region ***14*** after the necessary annealing process. This has adverse effects on the threshold voltage, since both its mean value and the dispersion of its values would increase. In fact, the peak concentration in the channel region ***14*** is of the order of approximately 10^{17} atoms/cm^3, while the surface concentrations in the contact area of the source ***5*** and body ***4*** regions must be higher than 10^{18} atoms/cm^3, as may be seen from the plot of the doping profiles along the directions A and B, shown in **FIGS. 1a and 1b**, respectively.

[11] The implantation dose further affects the defectiveness of the layers. In fact, as the dose increases, the likelihood of having precursor nuclei of extensive

defects increases. On the other hand, these cannot be eliminated or in any case reduced to acceptable levels by using intensive thermal treatment, since this treatment could damage other parts or other devices integrated in the same chip.

[12] In the above structure, the source regions ***5*** are obtained using an appropriate mask aligned inside the windows formed in the polysilicon layer. The above solution maximizes the channel perimeter (i.e., the facing perimeter between the source regions ***5*** and the channel regions ***14***) but may be used only when the distance between the gate regions is greater than 1 μm.

[13] However, in case of structures of submicrometric size, the distance between the gate regions tends to be as small as possible, lower than 1 μm. For such devices, it is no longer possible to use the structure of **FIG. 1**, and the electrical connection between the source and body regions is obtained in two different ways.

[14] For example, **FIG. 2** (where L < 1 μm) shows a solution wherein short-circuit is obtained through the use of an appropriate source mask. In practice, inside each body region ***4***, various source regions ***5'*** are formed, that, instead of extending in a continuous way along the edges of the gate regions ***10***, extend piece-wise in the direction Z for the entire width L (i.e., the width of the implantation windows of the body regions). In this way, body regions ***4*** have surface portions ***4'***, which face the top surface ***6*** of the body ***1*** and are electrically connected with the source regions ***5'*** through the metal layer ***13***. The above solution leads to a loss of channel perimeter even as much as 30% on account of the perimeter lost at the surface portions ***4'***. Furthermore, the problem of reducing the concentration of dopants in the source regions ***5'*** and hence of eliminating the problem of defectiveness is not solved.

[15] A second solution, illustrated in **FIG. 3**, consists in carrying out an etch for partial removal of the source regions in the region facing the surface ***6*** of the body ***1***. In practice, in the above solution, the source regions are implanted in the polysilicon over the entire area of the windows. Then, after forming spacers ***15*** on the sides of the gate regions ***10***, the portions of the source regions not covered by the spacers ***15*** are removed for a depth greater that that of the source junction ***5***.

At the end of the process, in each body region ***4*** just two thin source strips ***5"*** are present underneath the spacers ***15***, and the surface ***6'*** of the body ***1*** is no longer planar. In this case, etching of the silicon of the source regions ***5*** entails the need for contacting the source strips ***5"*** only along their vertical sides, with a considerable reduction in the contact area. Also in the above case, it is not possible to further reduce the defectiveness caused by the heavy doping of the source regions.

[16] In all of the above cases, the source metal region ***13*** extends along the entire side edge of the gate regions ***10*** and is insulated from these by the side portions of the intermediate-dielectric regions ***12*** (see **FIG. 1**) or by the spacers ***15*** (see **FIGS. 2 and 3**). This facing area, hereinafter referred to as "insulation region", is particularly critical and may be the cause of short-circuiting between the gate regions and the source regions on account of poor insulation. The insulation region plays an important role in the percentage of rejects since this percentage is proportional to the perimeter of the region, also referred to as "insulation perimeter". The presence of a high insulation perimeter in known devices is therefore disadvantageous.

[17] The aim of the invention is therefore to provide a MOS power device which will solve the problems outlined above.

SUMMARY

[18] According to aspects of the present invention a MOS power device and the manufacturing process thereof are provided, as defined in claims 1 and 8, respectively.

[19] In this way, the source and body regions are designed just considering the characteristics necessary for the formation of the channel region, which is now independent of the need for having surface concentrations compatible with good contact resistances. In practice, additional degrees of freedom for providing the channel region are obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

[20] For an understanding of the present invention, preferred embodiments thereof are now described, purely by way of non-limiting example, with reference to the annexed drawings, wherein:

[21] **FIG. 1** illustrates a perspective cross-section of a known MOS power device;

[22] **FIGS. 1a and 1b** illustrate doping profiles corresponding to the device of **FIG. 1**;

[23] **FIG. 2** illustrates a perspective cross-section of another known MOS power device;

[24] **FIG. 3** illustrates a perspective cross-section of a further known MOS power device;

[25] **FIG. 4** illustrates a perspective cross-section of a first embodiment of the invention, in a first manufacture step;

[26] **FIG. 4a**illustrates a doping profile corresponding to the device of **FIG. 4**;

[27] **FIG. 5** is a cross-section of the device of **FIG. 4**, in a subsequent manufacture step;

[28] **FIG. 5a** illustrates a doping profile corresponding to the device of **FIG. 5**;

[29] **FIG. 6** is a cross-section of the device of **FIG. 5**, in a subsequent manufacture step;

[30] **FIG. 6a** illustrates a doping profile corresponding to the device of **FIG. 6**;

[31] **FIG. 7** is a cross-section of the device of **FIG. 6**, in a final manufacture step;

[32] **FIGS. 8-12** are perspective cross-sections of a second embodiment of the invention, in successive manufacture steps; and

[33] **FIG. 13** illustrates a cross-section of a different embodiment of the invention.

DETAILED DESCRIPTION

[34] The following discussion is presented to enable a person skilled in the art to

make and use the invention. Various modifications to the embodiments will be readily apparent to those skilled in the art, and the generic principles herein may be applied to other embodiments and applications without departing from the spirit and scope of the present invention. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

[35] Initially (see **FIG. 4**), a body ***30*** of semiconductor material is formed comprising an N^+-type substrate ***31*** and an N^--type epitaxial layer ***32***, which form a drain region of the MOS power transistor to be fabricated. The body ***30*** has a top surface ***38***. On top of the body ***30*** gate oxide regions ***33*** and gate regions ***34***, of polysilicon, are formed in a known way. The gate regions ***34*** are separated from one another by windows ***40*** using an appropriate photolithographic process.

[36] Then, body regions ***35*** and thereafter source regions ***36*** are implanted in the windows ***40***. The body implantation is carried out, for instance, with boron, at a dose of 10^{13}-10^{14} at/cm^2 and the source implantation is carried out, for instance, with arsenic, at a dose of 2-5x10^{14} at/cm^2. **FIG. 4a**illustrates the doping levels thus obtained for the source region ***36***, the body region ***35*** and the epitaxial layer ***32*** (underneath the body region ***35***), along the direction B of **FIG. 4**.

[37] Then (see **FIG. 5**), a dielectric layer ***41*** is deposited (for instance, with a thickness of 500 nm), masked and etched so as to form first openings ***42*** in the regions where body contact regions are to be obtained. Then a P-type implantation is carried out, for instance, with BF_2 at a dose of 1-8x10^{15} at/cm^2 and an energy of 40-80 keV.

[38] In this way, the portions of the source regions ***36*** underneath the first openings ***42*** invert their conductivity type, forming P-type body contact regions ***43*** which extend as far as the body regions ***35*** (see, in particular, **FIG. 5a**, which illustrates the doping profile obtained, taken along direction B of **FIG. 5**). The body contact regions ***43*** present a higher conductivity than the body regions ***35*** and in absolute value also higher than the source regions ***36*** so as to invert them. Thereby, they enable electrical connection between the body regions ***35*** and the

surface ***38*** of the body ***30*** and reduce the direct voltage drop Vf of the body-drain internal diode (i.e., the diode formed by the regions ***35*** and ***32***).

[39] Next (see **FIG. 6**), using a mask (not illustrated), the source contacts are opened, and, at the same time and with the same process, the gate and edge contacts of the device are opened (not illustrated in the figure). In particular, in the dielectric layer ***41***, second openings ***45*** are made on top of the source regions ***36*** where the surface is to be enriched. In particular, the second openings ***45*** are made alternately to the first openings ***42***, as explained more clearly hereinafter. Next, an N-type implantation is carried out, for example of arsenic or phosphorus at a dose of $1\text{-}5x10^{15}$ at/cm^2 and an energy of 40-80 keV. In this step, the body contact regions ***43*** just obtained are covered by the mask for defining the openings ***45*** (not illustrated).

[40] Thus N^+-type source contact regions ***46*** are formed, that are alternated to the body contact regions ***43*** both along a same source region ***36*** (parallel to the direction Y in **FIG. 6**) and in a direction perpendicular to the preceding one (parallel to the direction X). The distance between the openings ***42*** and ***45*** and hence between the body contact regions ***43*** and the source contact regions ***46*** may be chosen as small as possible, for instance of 0.4-1 μm, so as not to jeopardize the strength of the MOS device on account of turning-on of the parasitic transistor formed by the source ***36***, body ***35*** and drain (epitaxial layer ***32***) regions.

[41] After thermal activation of the dopants at a low temperature (800-950°C), in a cross section taken along the direction C, the doping levels illustrated in **FIG. 6a** are obtained.

[42] Finally, on the entire surface of the wafer a source metal region ***50*** is deposited, which fills the first and second openings ***42***, ***45*** and hence alternately contacts the body contact regions ***43*** and the source contact regions ***46***. Furthermore, the bottom surface of the body ***30*** is covered by a rear metal region ***37***. The final structure of **FIG. 7**is thus obtained.

[43] The technique may be extended also to the case of submicrometric devices, for which the size of the opening of the windows ***40*** between the gate regions ***34***

does not enable opening of contacts using traditional techniques. In this case, a further mask is provided for separating contact opening on the gate regions from contact opening on the source and body regions, which are obtained by anisotropically etching an insulating layer forming a spacer in a self-aligned manner, as described hereinafter with reference to **FIGS. 8-12**.

[44] For the above devices, the process comprises (see **FIG. 8**), after deposition of a polysilicon layer ***34***, deposition of a first dielectric layer ***60*** (for instance, of 500 nm), and definition of the first dielectric layer ***60*** and of the polysilicon layer ***34*** for forming the gate regions ***34*** overlaid by the dielectric regions ***60***. Moreover, the windows ***40*** are formed through which the body regions ***35*** and source regions ***36*** are implanted.

[45] Next (see **FIG. 9**), a second dielectric layer ***61*** (for instance, of 500 nm) is deposited, and (see **FIG. 10**) a first photolithography is performed for forming the second openings ***45*** on top of the source regions ***36***. To this end, a first resist mask ***62*** is formed, and the second dielectric layer ***61*** is anisotropically etched so as to form spacers ***70***, on the side of the gate regions ***34*** exposed by the second openings ***45***. After removal of the first resist mask ***62***, a second photolithography is performed (see **FIG. 11**) for opening contacts on the gate regions. For this purpose, a second resist mask ***63*** is formed, having third openings ***71*** in regions of the device where no active areas are present, and a thick field-oxide layer ***72*** extends underneath the polysilicon layer ***34***. The second dielectric layer ***61*** and the first dielectric layer ***60*** are etched at the third openings ***71***. Then the second resist mask ***63*** is removed.

[46] After implantation of the source contact regions ***46***, through the second openings ***45***, and of the gate contact regions ***65***, through the third openings ***71*** (see **FIG. 12**), the following steps are carried out: a third photolithography for forming the first openings ***42***, without subsequently removing the mask; implantation of the body contact regions ***43***; removal of the mask of the third photolithography; activation of the dopants; and the usual operations for forming metal interconnects and back end. The structure illustrated in **FIG. 12** is obtained,

where the surface metal layer has not been represented for clarity.

[47] **FIG. 13** illustrates a different embodiment wherein the body contact regions, instead of being formed by implanted regions that invert the source regions ***36***, are made by anisotropically etching the source region 36 which, starting from the surface 38, reaches the body regions ***35***.

[48] In this way, the source metal layer 50 contacts the body regions ***35*** in depth, where the concentration of dopant is normally higher (see **FIG. 1b**). For this purpose, using the known shallow-trench technique and removing part of the source regions ***36*** underneath the first openings ***42***, cavities ***55*** are formed, which reach the body regions ***35***. In this way, when the source metal region ***50*** is deposited, this fills the cavity ***55*** underneath the first openings ***42*** and, on the bottom of the cavities ***55***, contacts the body regions ***35*** with portions ***56***. In practice, in this solution, the source metal region ***50*** forms the body contact regions.

[49] The advantages of the device and the process described are outlined hereinafter. First, it is possible to enrich the contact regions (source contact regions ***46*** for all the embodiments illustrated, body contact regions ***43*** for the embodiments of **FIGS. 7 and 12**), without affecting the channel regions ***47*** of the device. In this way, it is possible to reduce the output resistance and the voltage drop Vf on the body-drain parasitic diode.

[50] The above enrichment may take place without affecting the dose and the implantation conditions of the source ***36*** and body ***35*** regions, which may be optimized independently of the other regions. In this way, it is possible to reduce the problem of defects and improve the electrical yield. This is also made possible by the fact that the usual lateral distances between the body and source contact regions ***43***, ***46*** and the edge of the gate regions ***34*** (which is greater than 0.15 μm) and the low thermal budget used for activating the dopants are sufficient to prevent the high dose introduced into the body and source contact regions ***43***, ***46*** from affecting the concentration of the dopants in the body region ***35*** at the channel ***47*** (see **FIG. 7**).

[51] A further improvement of the electrical yield and a reduction of the rejects are obtained thanks to the reduction of the insulation perimeter. In fact, the source metal region ***50*** does not face the side edges of the gate regions in a discontinuous way, and not throughout the length of the source regions ***36***. In this way, for a same channel perimeter, there is a smaller insulation perimeter.

[52] The reduction in the implantation dose of the source regions ***36*** enables an improvement of the strength of the device thanks to the reduction of the gain of the source-body-drain transistor.

[53] Finally, it is clear that numerous modifications and variations may be made to the device and the process of manufacture described and illustrated herein, all falling within the scope of the invention, as defined in the annexed claims.

[54] For example, although an N-channel MOS device has been described, the described embodiments of the invention may be applied also to P-channel devices, changing the dopant agents for the various regions (phosphorus or arsenic for body enrichment and BF_2 or boron for source enrichment). Opening of the contacts on the polysilicon of the gate regions may be carried out together with that of the source or body regions according to the type of doping.

[55] The succession of steps followed for obtaining the body contact regions ***43*** and the source contact regions ***46*** may be inverted with respect to what is described herein.

[56] In addition, as is shown in **FIG. 13**, the body enrichment may be replaced with a silicon etching.

[57] Finally, although the gate regions 34 have been represented as separate regions, they are generally connected together in such a way as to form a grid with rectangular or square openings in which the body regions ***35*** and source regions ***36*** are made, which thus may have a strip-like shape or a square shape. In addition, the embodiments of the invention also apply to other types of layouts; for example, also the body regions ***35*** may be formed by strips connected together at one end or both ends, as likewise the source regions.

[58] The MOS power devices described in the above embodiments of the

present invention may be used in a variety of different types of electronic systems, such as computer, communications, power supply, and control systems.

[59] From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention.